Exercise 7: Photodetectors

Location: MED 2 117

Contact: Cristian de Giorgio, cristian.degiorgio@epfl.ch

1. Summary

In this exercise, you will continue with the device characterization by working on photodetectors (or phototransistors) based on MoS_2. These devices are the same transistors used in exercise 5. Exposing them to light results in the generation of extra charge carriers in the semiconducting channel, resulting in additional current, compared to the current in a transistor kept in dark. This effect can be used to detect light. The direct band gap of MoS_2 and related materials together with the atomic scale thickness and high current on/off ratio make them interesting for this application.

The main goal of this exercise is to carry out basic photodetector characterization, identify the main effects of exposing the transistor to light on its electrical characteristics and calculate the responsivity of the devices.

2. Background

2.1. Phototransistors based on 2D semiconductors

A phototransistor is simply a transistor exposed to light on purpose, Figure 1a. Semiconducting devices are in general light-sensitive and the absorption of photons in the transistor device channel generates free charge carriers which modifies the electrical characteristics of the device. Unless you are actually interested in using the devices as photodetectors, this can be a problem since it would result in difficult to reproduce electrical characteristics. Because of this transistors and integrated circuits are normally sealed in opaque packages.

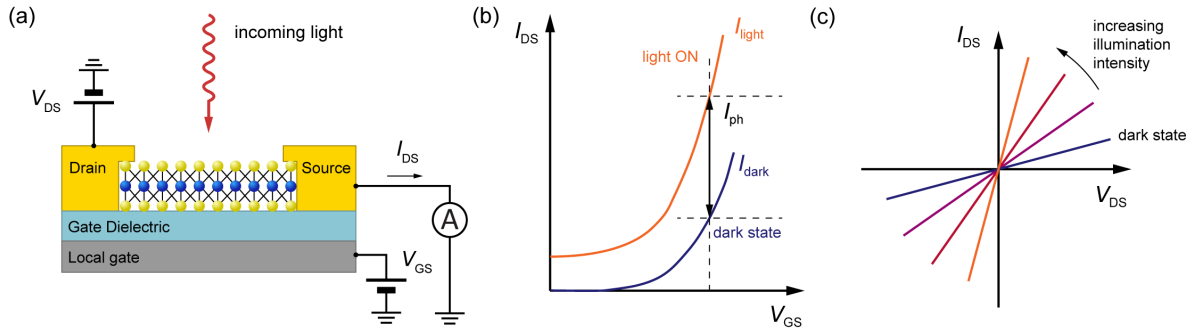


Figure 1. (a) Schematic of a 2D-material based phototransistor, with electrical connections. (b) Exposing the transistor to light results in increased current. (c) Exposure to light changes the electrical resistance of the device.

Figure 1b show the gating characteristics of the 2D FET. In the absence of illumination, the device has a typical gating ($I_{DS} - V_{GS}$) characteristic and the application of a bias voltage V_{DS} will result in current, that we call in this case dark current (I_{dark}). When the device is illuminated, photons with the energy above the band gap of the semiconducting material can be absorbed, resulting in the generation of electron-hole pairs. The presence of a direct band gap in 2D semiconductors such as MoS_2 makes this process in principle more efficient than for

materials with an indirect band gap such as for example Si. In the presence of a bias voltage the electrons and holes are separated and the device current increases, Figure 1b. The difference between the current under illumination I_{light} and the dark current I_{dark} is the photocurrent: $I_{ph} = I_{light} - I_{dark}$, Figure 1b. The photocurrent in principle depends on both the bias and the gate voltage. The extra charge carriers and the photocurrent effectively decrease the resistance of the device. This can be seen also in the biasing ($I_{DS} - V_{DS}$) characteristic, Figure 1c, as an increase in the slope of the $I_{DS} - V_{DS}$ curves.

One of the most important figures of merit for a photodetector is the photoresponsivity (R), defined as the ratio of the photocurrent I_{ph} and the incident illumination power P_{inc}:

$$R = \frac{I_{ph}}{P_{inc}} \tag{1}$$

and is expressed in units of A/W.

This behaviour of photodetectors can be explained by a simple energy band diagram, Figure 2, with a Schottky barrier at the contacts of Φ_B, Fermi level E_F, conductance and valence band edges at E_C and E_V. In the absence of light and voltages applied to the device, the photodetector is in the equilibrium state (Figure 2, left). Illuminating the device with a light with wavelength above the optical band gap of MoS_2 (around 647 nm), results in the generation of electron-hole pairs, which can move under the application of a drain source bias. The electron-hole pairs are in principle generated also when the device is in the OFF state, characterised by $V_{GS} < V_{TH}$ where V_{TH} is the threshold voltage of the transistor. The resulting photocurrent is then added on top of the OFF-state current. As the device is turned on, both intrinsic and photocurrent increase, in part also because the Schottky barriers at the contacts are reduced, allowing more efficient charge carrier extraction.

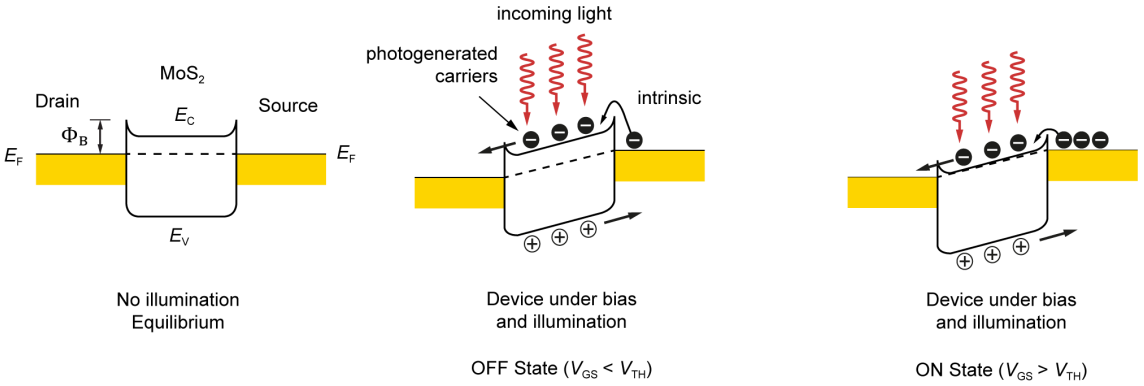


Figure 2. Band diagram of the MoS_2 photodetector. Left: equilibrium state with no voltages applied and no illumination. Middle: OFF state of the transistor, with background current given by the OFF-state current of the device. Illumination results in the generation of extra carriers which are extracted, resulting in increased current. Right: ON state of the transistor. The photocurrent is added to a larger background current.

The device can in principle be operated in either ON or OFF states: operating in the ON state results in a higher photocurrent and responsivity. Operating in the OFF state brings the advantage that the I_{dark} in this range of gate voltages is very low, corresponding to the I_{OFF} of the transistors. In situations where we would like to detect weak signals, the photocurrent has to be above the noise level of the dark current, so lower I_{dark} also means lower noise. This is where the high ON/OFF current ratio of 2D semiconductor transistors and the efficient electrostatic coupling come in play.

Not all the charges generated by illuminating the channel get extracted in the form of photocurrent, some of them also get trapped in defect states either in the channel, gate dielectric or the interface. These trapped charges then effectively gate the conductive channel and in this way also contribute to modifying the electrical resistance of the material. Since some of these trap states can have long lifetimes, on the order seconds, this trapping can slow down the device bandwidth of the device. Its influence on the electrical properties can be seen by measuring the gating characteristics of the device. While regular photoconductive effect results in a vertical shift of the $I_{DS} - V_{GS}$ characteristic, photogating is manifested in a horizontal shift of the curve.

2.2. Wire bonding and packaging (repeated from Exercise 5)

In order to connect the contact pads on the devices with the external electronics, the TA used the method called wire bonding and a wire bonder, Figure 3a. This is a common method for connecting integrated circuits to packages such as the one used in this exercise and shown on Figure 3b.

The wires used to make the connection have a diameter of 25 µm (for comparison, a typical diameter of a single hair is ≈ 80-100 µm) and are made of an alloy of aluminum and silicon (1%). During the wire bonding process, the user manipulates the tool wedge under a microscope. This wedge resembles a needle in a sewing machine with the thin wire in place of a thread. The hand motion of the operator is de-multiplied by a factor of 10, so that regular movements of the hand can be used to manipulate the tool under the microscope with sufficient precision. Once the sensor inside the tool detects mechanical contact with a contact pad, a short ultrasonic pulse is emitted which bonds the wire with the contact pad either on the chip or the package. The process is quite straightforward but requires some skill since a common beginner mistake is to apply too much pressure on the tip which can result in the failure of the insulating film under the contact pads and an electrical short circuit between the source/drain electrodes and the gate.

(a) (b)

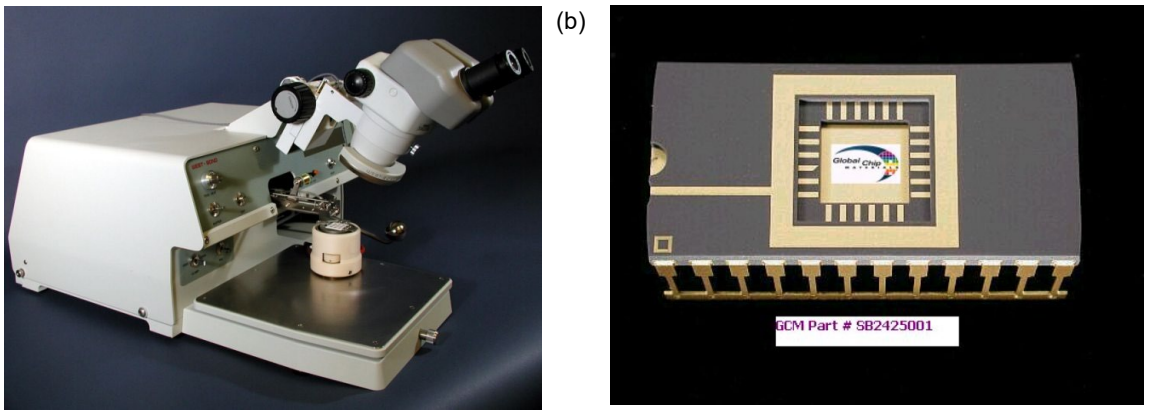


Figure 3. (a) Photo of a manual wire bonder from the company Westbond, used for preparing the chip using in this exercise. (b) Ceramic (mostly) chip package made by the company Kyocera, used in this exercise.

2.3. Electrostatic discharge (repeated from Exercise 5)

Electrostatic discharge (ESD) is an event in which static electricity from for example your clothes can be released. ESD can destroy delicate electronic devices such as the ones used in

this and subsequent exercises. You have probably been zapped by such discharges when removing clothes for example. Such discharges involve potentials on the order of 100 V or even more (but the amount of charge is small so you do not get electrocuted). Smaller events, on the order of 10 V happen quite often but are normally not perceived. Those are still sufficient for destroying the devices by for example touching the chip with bare hands. Common methods or protection involve grounding equipment or yourself through a ~ 1MΩ which decreases the currents associated with ESD but allows the efficient removal of charges.

In order to protect the devices from ESD, you will need to take several precautions. You will attach an antistatic wristband, which will effectively ground you. It then advised to handle the chips, wires, electrical cabling etc. with the hand on which you are wearing the bracelet. The work area is also going to have a grounded mat and the chip is also stored in an ESD-safe box, made of a conducting polymer.

3. Description of the equipment used

Overview of the setup

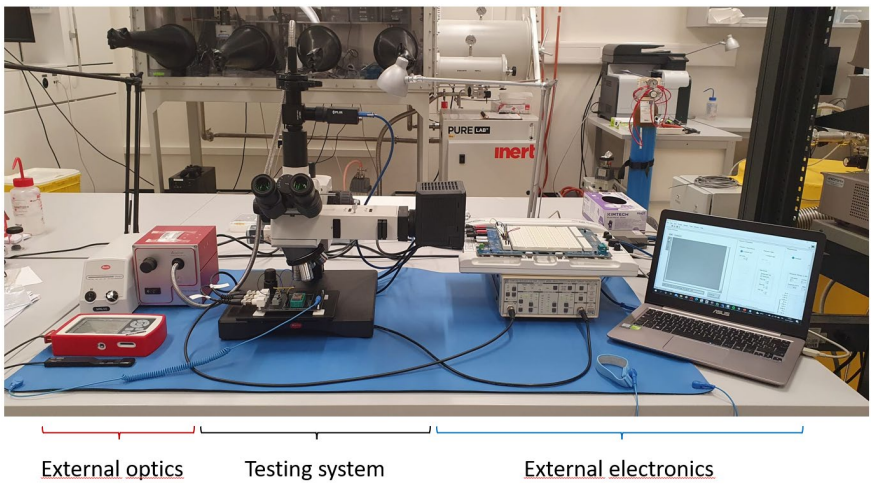


Figure 4. Overview of the experimental setup used in this exercise.

External optics

These parts of the setup comprise the power supplies for the light sources and the power meter. We distinguish between two light sources. First is the power supply for the main microscope light source which is used for illuminating the sample, labelled 1 on Figure 5. The corresponding light source is the lamp in a black housing, located on the side (sometimes also back) of the microscope. It is strong enough for regular imaging. Since we would like to also modulate more strongly the intensity of the light interacting with the photodetector, we use an additional light source, in the form of a lamp, coupled to a fiber optic bundle (2 on Figure 5). The powermeter (PM 100D from Thorlabs, with a silicon detector S130C) is used to calibrate the light sources for accurately measuring the photoresponsivity of the devices.

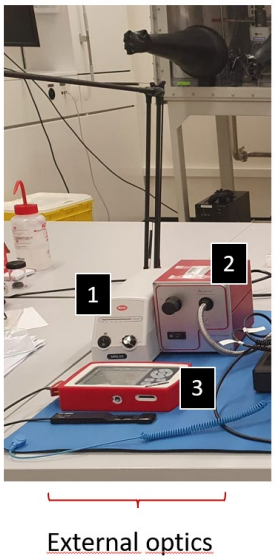


Figure 5. Overview of the external optics part. 1: power supply for the white light source mounted on the microscope. 2: light source used to illuminate the phototransistor via an optical fiber bundle. 3: optical power meter.

Overview of the testing system

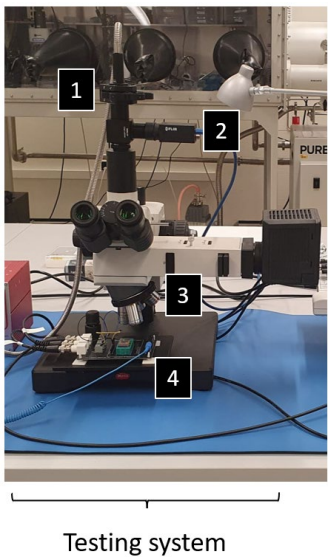


Figure 6. Overview of the optical microscope with attached components. 1: filter wheel. 2: camera. 3: objectives, 4: test board.

The c-port of the microscope contains an assembly of components that comprises the port of the optical fibre bundle illumination and the filter wheel (label 1 on Figure 6). The filter wheel contains several neutral density filters. These filters reduce the intensity of incoming light, affecting all visible light wavelengths equally. They will be used to controllably and reproducibly modulate the light intensity during the power-dependent measurements. ND filters are usually labelled as NDn where 1/n corresponds to the fraction of the light which is

transmitted. For example, ND4 transmits ¼ of incoming light intensity. The camera (label 2 on Figure 6) is used to record photos and videos from the microscope using the connected laptop.

Test board

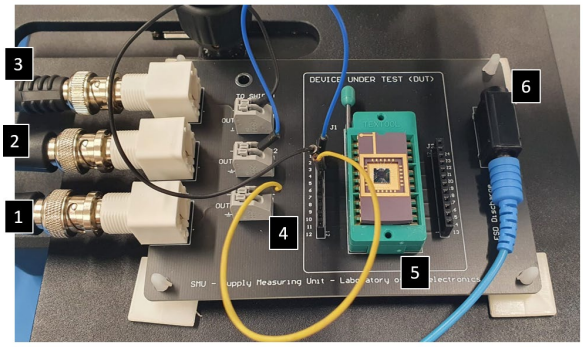


Figure 7. Test board with the connections. 1: Channel 1 (V_{ds}), 2: Channel 2 (V_{gs}), 3: BNC connection to the input of the SRS 570 preamplifier for measuring I_{ds}. 4: connectors. 5: ZIF socket with chip. 6: connector for the ESD bracelet.

The test board allows us to interface the devices mounted in the chip package with the external electronics. The devices are also exposed to light from the microscope and can be manipulated under the objective using an x-y translation stage.

Overview of external electronics

We will use a combination of a DAQ board and a current preamplifier for applying the voltages to the photo transistors and measuring the resulting current.

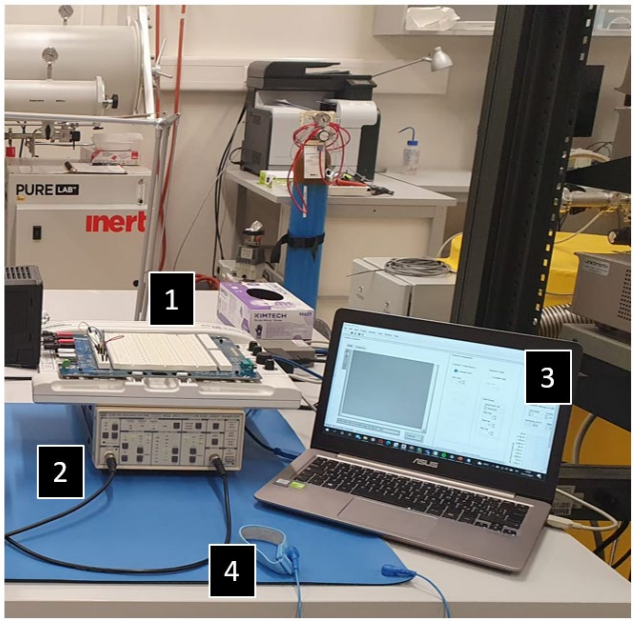


Figure 8. Overview of the part of the setup used for electrical measurements. 1: NI-ELVIS board used for generating the voltages applied to the transistor and for measuring the current via the current preamplifier. 2: SR570 current preamplifier is used to measure the I_{ds} current converted to voltage read by NI-Elvis DMM. 3: laptop running the LabVIEW code for the data acquisition. 4: Grounding bracelet.

AD/DA DAQ board - National instruments Elvis board

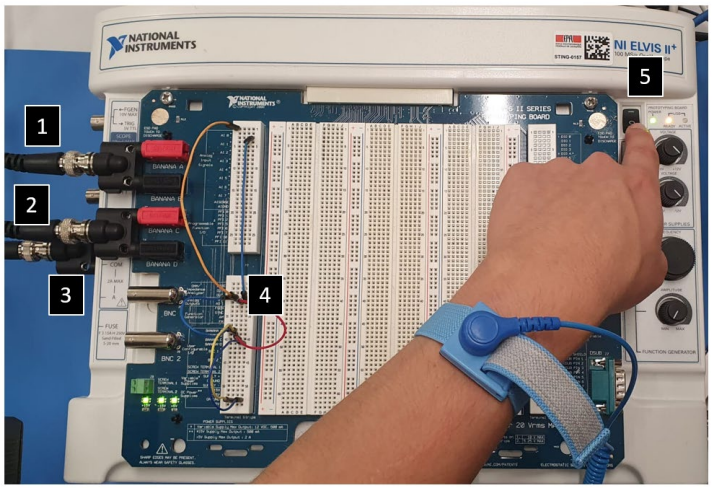
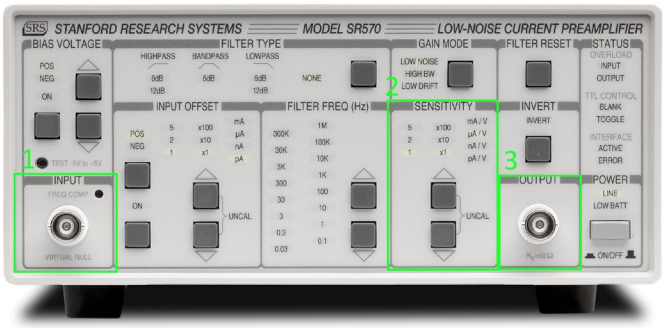


Figure 9. ELVIS board overview. 1: Channel 1 – V_{ds} (analog output 1). 2: Channel 2 – V_{gs} (analog output 2). 3: DMM for measuring the SR570 output voltage (amplified Ids from SRS Preamp). 4: Connections from analog outputs to analog inputs to observe signals on LabVIEW. 5: Main on/off switch for the ELVIS board.

We will use the National Instruments ELVIS board to generate the analog signals and to sample the output of the current preamplifier. The specialty of the ELVIS board is the integration of a prototyping board with a National Instruments acquisition board capable of acting as a wide variety of instruments. The board has eight analog input channels for converting analog to digital signals (labeled AI 0 to AI 7 on the board) and two analog output channels for DA conversion (AO 0 and AO 1). These can be connected to different rows on the prototyping board and to various physical connectors (banana, BNC, DB9) using the provided jumper wires (4 on Figure 9). These have already been connected by the assistant so that the analog output signals generated by the ELVIS DA converter for the V_{DS} and V_{GS} voltages are supplied to BNC cables labelled (1) and (2) on Figure 9 while the AD converter is connected to connector (3) which samples the output voltage from the current preamplifier.

Current preamplifier – Stanford Research Systems SR570

(a)



(b)

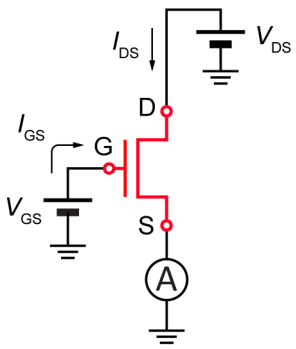


Figure 10. (a) Front panel of the SR 570 current amplifier. 1: Input BNC, 2: Sensitivity selector, 3: output BNC. (b) connection schematic for the exercise. The voltage sources correspond to the analog outputs of the ELVIS DAQ board. The current preamplifier is connected as an amperemeter, in series with the device.

In this exercise, we will use a scientific laboratory-grade current-voltage converter (also referred to as a current preamplifier), Figure 10a, made by company Stanford Research Systems. This is an instrument that converts low-level currents on the input into voltages on the output. The sensitivity is selected on the "Sensitivity" section of the front panel (2 on Figure

10a. The output voltage is in the −10 V, 10 V range. This particular model is very popular in the scientific community because it was one of the first of its type to feature a built-in battery which allows it to operate independently of the electrical supply lines, resulting in reduced noise (when required by the experiment).

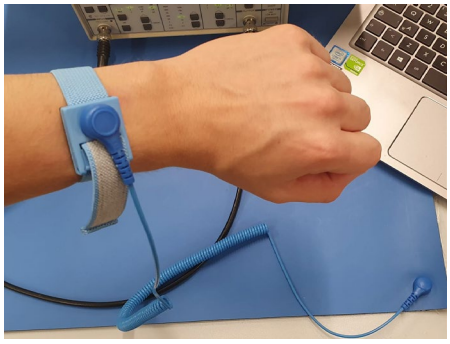
The instrument is connected in the circuit as an amperemeter (Figure 10b) in such a way the input of the current preamplifier corresponds to a point in circuit that would otherwise be grounded. The ground is then provided by the rest of the circuit via the shield of the BNC connector.

4. Description of experiments and tasks

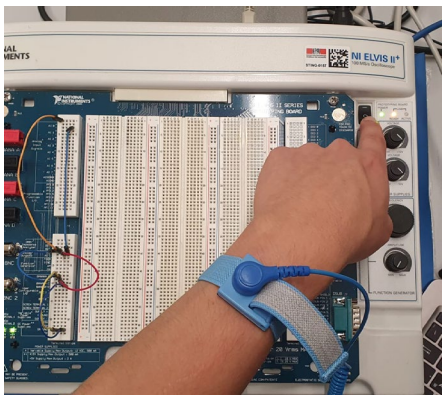
Following is the overview of the tasks and operations to be carried out in this exercise. The main goal is to perform electrical characterization of MoS_2-based transistors operating as photodetectors.

4.1. Setup: preparing the external electronics

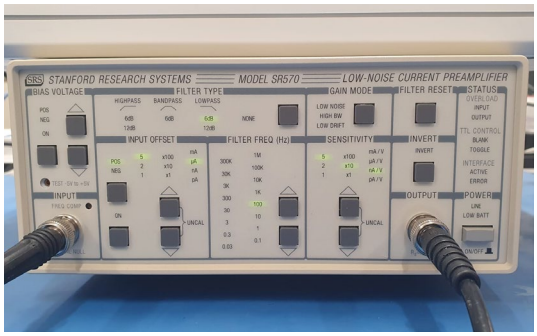
1. Ground yourself through the ESD bracelet.



2. Turn on the NI ELVIS board

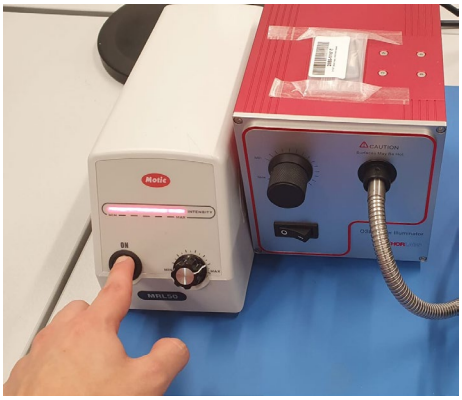


3. Set up the current preamplifier

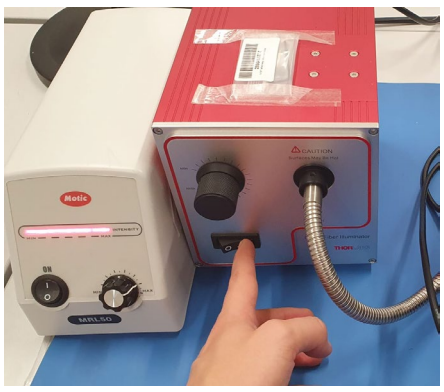


4.2. Prepare the external optics

4. Turn on the white light source

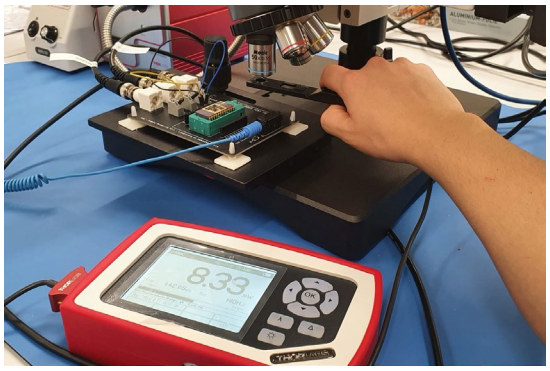


5. Turn on the fiber-coupled light source

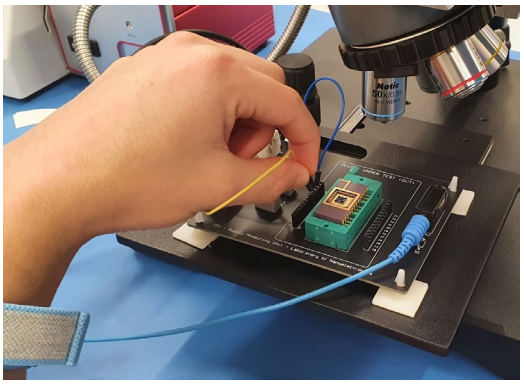


6. Adjust the filter wheel position

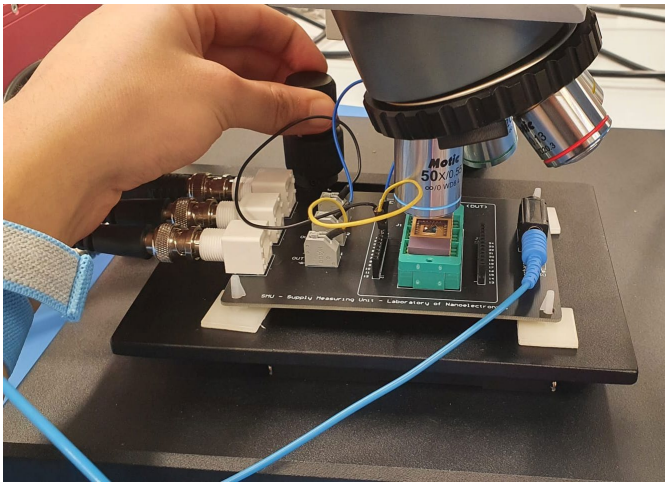
7. Measure power with the power meter. This needs to be repeated for the different ND filters used for this exercise.



8. Lock the chip in the ZIF socket, connect the jumpers to the desired positions



9. Use the stage positioners to locate the sample under the objective



4.3. Connecting an individual phototransistor device

We will use for this exercise the same transistors used in Exercise 5 on transistors and TLM. The chip contains two sets of devices outlined on Figure 11. The contact pad numbers correspond to the legs on the chip carrier and the pins in the test board.

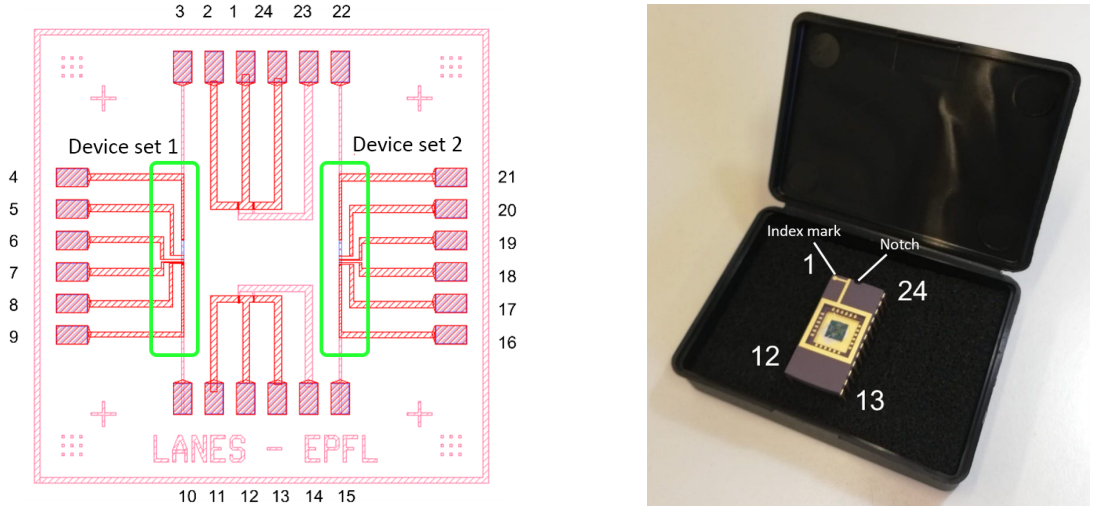
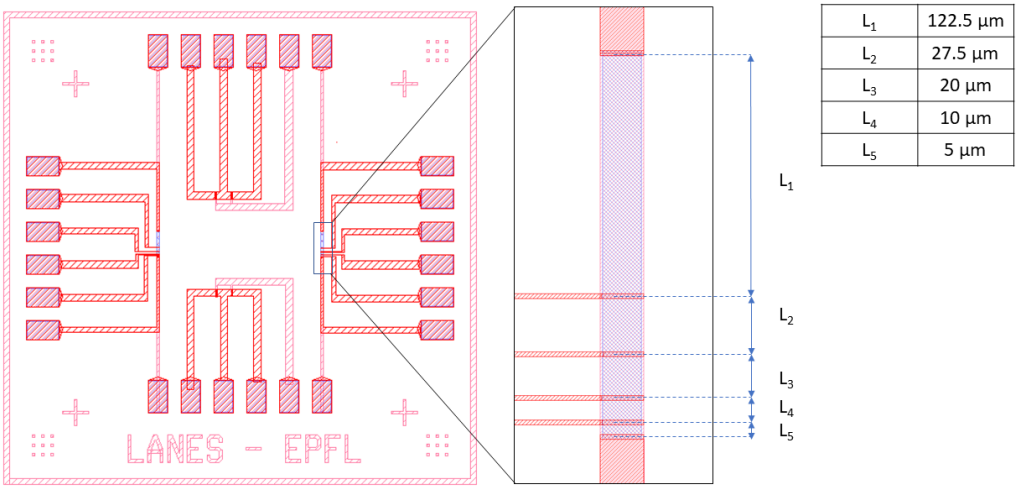


Figure 11. Left: schematic drawing of the device layout, with the corresponding pin numbering. There are two sets of transistor devices with varying channel lengths. Device set 1 has the local back-gate connected to pins 3 and 10. Pins 4-9 correspond to electrical contacts. Neighboring pairs can be used as drain and source electrodes. Device set 2 has the local back-gate connected to pins 15 and 22. Pins 16-24 correspond to electrical contacts that can be used as drain and source electrodes. Right: photograph of a chip carrier package. The pins are numbered in a counter-clockwise direction, starting from pin 1 at the index mark (rectangle close to a corner of the chip).

By manually connecting the wires between the jumpers and the pins you can access the different devices on the chip.

The dimensions of the transistors in the device set 2 are shown in Figure 12, device set 1 has the same dimensions.



L_1	122.5 µm
L_2	27.5 µm
L_3	20 µm
L_4	10 µm
L_5	5 µm

Figure 12. Channel lengths for the transistors in the device set 1. Both transistor device sets (1 and 2) have the same dimensions. The channel width for all devices is 20 µm.

4.4. Familiarize yourself with the software interface

We will use a program in Labview for controlling the sourcemeter and measurement acquisition, with the interface shown in Figure 13.

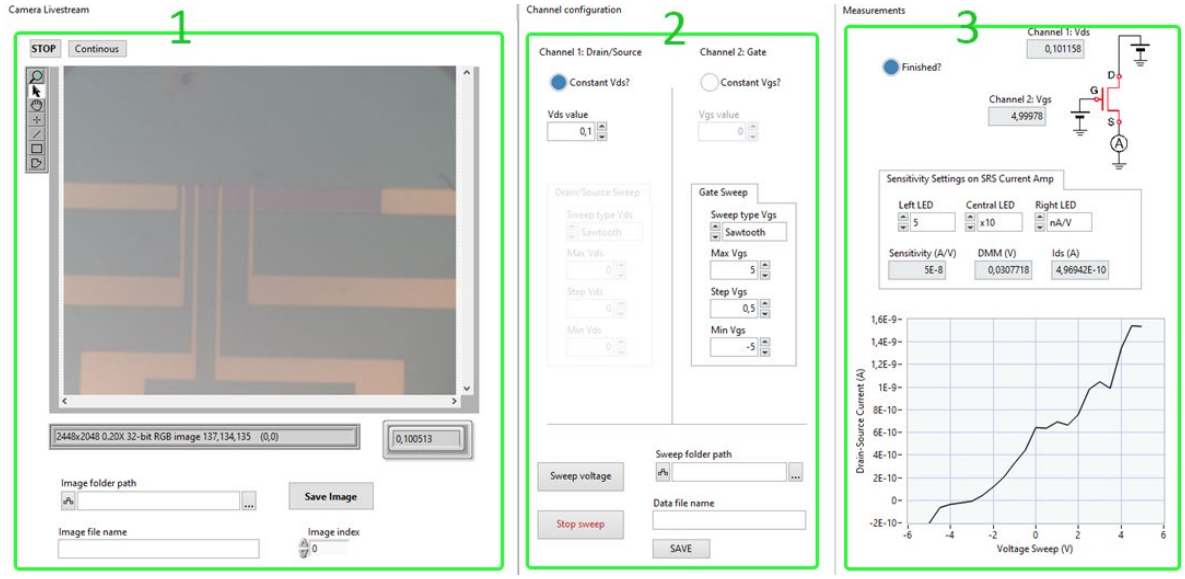


Figure 13. Interface for the data acquisition software used in this exercise.

Its main parts are:

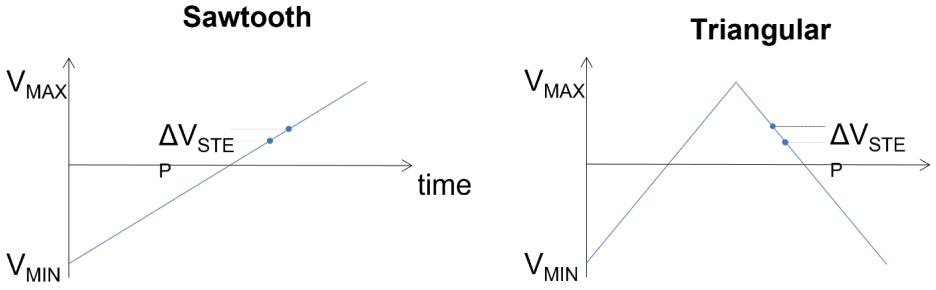
1. Camera livestream
2. Channel configuration
3. Measurement setup

Camera livestream (1)

This part of the GUI shows the live-view from the camera attached to the microscope, it can be used to quickly locate a region of interest and focus the view. The images can also be saved.

Channel configuration (2)

In this part of the GUI, you define the voltages applied ot the device and the voltage sweep type. You can perform 2 types of sweeps, sawtooth or triangular:



When the configurations are ready, press the button "Sweep voltage" to start the sweep.

Measurements

Here, you can manually enter the sensitivity of the SRS current amplifier and preview the results of the volage sweep.

4.5. Perform device characterisation

1. **Dark state characterisation of the device.** For one of the FGFETs, set the bias voltage to $V_{DS} = 1$ V and cycle the gate voltage V_{GS} in the -10V , 10V range while recording I_{DS} vs V_{GS}.
2. **Measurements under different illumination intensities.** Using the ND filters, set 3 different levels of illumination intensities. Measure the illumination intensity using the optical power meter and estimate the optical power received by the devices by scaling the total measured power to the surface area of the device. For each of these 3 different light levels, measure the gating ($I_{DS} - V_{GS}$) and biasing ($I_{DS} - V_{DS}$) characteristics.

5. Questions for the report

In the report, please show and discuss the following:

1. Show sets of gating ($I_{DS} - V_{GS}$) and biasing ($I_{DS} - V_{DS}$) characteristics for the dark state and different illumination intensities.
2. Calculate and discuss the responsivity R of the photodetector as a function of gate voltage.
3. Calculate and discuss the responsivity R of the photodetector as a function of gate light intensity, for a constant value of gate voltage.